FLUID EJECTION DEVICE

BACKGROUND

[0001] A fluid ejection device, such as an ink jet printhead, may comprise a substantially linear column of firing chambers with firing resistors. The firing resistors typically have associated drive circuits with drive transistors which energize the resistors to expel fluid from the chamber through an orifice or nozzle. The drive transistors are arranged in a column along side of and substantially parallel with the column of firing resistors. Although a vertical column of resistors is substantially linear, some resistors may be offset horizontally as disclosed, for example, in US Patent 5,635,968.

[0002] The fabrication of a fluid ejection device may include a surface etch using an etchant such as TMAH. The etch takes place after the transistors have been fabricated on the substrate. The transistors include contacts which provide an electrical contact to the substrate through vias in an insulation layer. During a subsequent etch, the etchant attacks, i.e. etches away additional portions, of the substrate through openings in the insulation layer through which the contacts pass. The attack often occurs through pinholes located in a passivation layer above the insulation layer in the region of the contacts.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Features of the invention will readily be appreciated by persons skilled in the art from the following detailed description of exemplary embodiments thereof, as illustrated in the accompanying drawings, in which:

[0004] FIG. 1 is a cutaway view of an exemplary embodiment of a fluid ejection device.

[0005] FIG. 2A illustrates a plan view of an exemplary embodiment of a layout of a drive transistor and firing resistor.

[0006] FIG. 2B illustrates a cross-sectional view of the exemplary embodiment of FIG. 2A.

[0007] FIG. 3 illustrates an exemplary embodiment layout of transistors and power busses of a fluid ejection device.

DETAILED DESCRIPTION OF THE DISCLOSURE

[0008] In the following detailed description and in the several figures of the drawing, like elements are identified with like reference numerals.

[0009] FIG. 1 illustrates an exemplary embodiment of a fluid ejection device 1 in a simplified, partially broken-away, diagrammatic isometric view. The fluid ejection device may comprise a silicon substrate 2. Formed on the substrate, for example by thin film layers, are rows of drive transistors 3 with associated decode logic 4. The drive transistors 3 energize associated, respective resistors 5 or heating elements, however any structure that is capable of heating is capable of being utilized as a resistor. Electrical traces and vias 6 couple the drive transistors 3 to the resistors 5 and address busses 7. Disposed above the drive circuits are primitive power busses or power traces 8. Each primitive power buss 8 is electrically connected to a plurality of drive transistors and provides a common voltage, which acts as a power source, to all of the transistors to which it is connected. The group of transistors 3 and associated, respective resistors 5 powered by a given power buss 8, along with associated firing chambers 91 and nozzles 11, comprise a primitive group 81.

In the exemplary embodiment of FIG. 1, two columns of firing resistors are separated by a fluid feed slot 21.

[0010] A barrier layer 9 defines a plurality of firing chambers 91, each associated with an individual firing resistor 5. An orifice layer or orifice plate 10 has nozzles 11 formed through the plate. Fluid fed from the feed slot 21 into a firing chamber 91 is heated by a resistor 5 when its associated transistor 3 fires, thereby heating the fluid and expelling some of the fluid out through an orifice 11. In the case of an ejection device which is an inkjet printhead, expelled ink may be propelled onto a media such as paper, mylar, fabric, or other media.

[0011] FIGS. 2A and 2B illustrate an exemplary embodiment of a drive transistor 3 and resistor 5. A drive transistor 3 may comprise at least a polysilicon gate portion 31 disposed over a substrate 2. The polysilicon gate portion 31 may be disposed over a gate oxide layer 34 between the substrate and the polysilicon gate portion. Contacts 41 extend through an insulation layer 35 and may contact drain regions 32 or source regions 33, but not substrate 2. The insulation layer 35 may be disposed on the substrate and may be disposed over the polysilicon gate portions and may comprise phosphosilicate glass (PSG). The contacts may comprise PSG contacts, diffusion contacts, drain contacts, source contacts, poly contacts and/or other contacts.

[0012] FIG. 3 illustrates an exemplary embodiment of a layout of transistors and power busses in a fluid ejection device 1. The fluid ejection device has a plurality of firing resistors 5 and a plurality of associated drive transistors 3. For simplicity, the electrical traces and other features of a drive circuit are omitted from the illustration. For convenience, the columns may be considered as being arranged in a substantially vertical direction, but other orientations are possible and may be utilized with layouts and device structures described herein. For example, the resistors 5 and transistors 3 could be arranged in

rows. The resistors 5 in the column may be evenly and uniformly spaced along the column. For instance, each resistor may be uniformly spaced, centerline-to-centerline, a vertical distance V1 from adjacent resistors along the column. In an exemplary embodiment, the resistors may be spaced, centerline-to-centerline, about 84.7 um apart. The resistors may have dimensions of about 28.6x14.2 um and may comprise split resistors with two halves separated by a gap of about 2um. The centerline referred to in this exemplary embodiment is the horizontal line running through a point halfway between the uppermost extent of a resistor and the lowermost extent of that resistor. In this embodiment, the resistors are illustrated as of a rectilinear shape. In other embodiments, a different shape may be employed and/or a different centerline may be selected. Although the resistors 5 in FIG. 3 are shown in a column, in certain, alternative embodiments, the horizontal placement of some resistors along the column may be offset to one side or the other. In some embodiments, the resistors may not be uniformly spaced.

[0013] In this embodiment, the resistors 5 and transistors 3 of a column are arranged in primitive groups 81. The resistors 5 and associated, respective transistors 3 in a primitive group are each electrically connected to a common one of the plurality of power busses 8. In FIG. 3, the perimeter 82 of the areas covered by power busses 8 are designated with dotted lines. In an exemplary embodiment, a power buss 8 may be disposed as a conductive layer over the drive transistors 3, as shown in FIG. 1. The power busses 8 may comprise an electrically conductive layer which may comprise tantalum, gold, other metal, other conductive material, or alloys thereof. In an exemplary embodiment, the power buss 8 may have dimensions of about 2177.5x198 um. A primitive group 81 may comprise 26 resistors 5 and 26 transistors 3.

[0014] The transistors may comprise a polysilicon gate portion 31 and contacts 41. In an exemplary embodiment, the contacts 41 lying between adjacent

transistors 3 within a primitive group 81 may act as a contact 41 for the transistors on either side of the contacts 41. An exemplary transistor has a vertical height H. The height H may be defined between the outermost contacts which provide the electrical connection to the polysilicon, or the doped polysilicon or silicon substrate, as appropriate. The transistors 3 may be placed close together. Contacts 41 may be shared by adjacent transistors 3. In an exemplary embodiment, a transistor 3 may have dimensions of about 77.5x198 um.

[0015] The height of a transistor may be selected, in part, to provide desirable transistor efficiency. The overall efficiency of a transistor may be related, in part, to the surface area covered by the transistor. A transistor with a height H which is too small, may have an impedance which is too high for desired efficiency of operation. In FIG. 3, the transistors are shown, by way of example, with four polysilicon legs. The efficiency of the transistor may be increased, for example, by adding additional legs and corresponding additional drain and source regions and contacts as appropriate. In an exemplary embodiment, a transistor with desirable efficiency characteristics may have as many as eight polysilicon gate legs or more.

[0016] In an exemplary embodiment, transistors of a given primitive group may be uniformly spaced along the column of transistors. In FIG. 3, for example, the transistors 3 within a primitive group 81 are spaced, centerline-to-centerline, a distance V2 apart from adjacent transistors of the primitive group. In an exemplary embodiment, the transistors within a primitive group may be spaced, centerline-to-centerline, about 84 um apart. The spacing of the transistors 3 of a primitive group may be different from the spacing of the resistors of a primitive group. In FIG. 3, for example, the separation distance V2 of the transistor spacing is smaller than the separation distance V1 of the resistor spacing. The centerline referred to in this exemplary embodiment is the horizontal line

running through a point halfway between the uppermost extent of the transistor and the lowermost extent of the transistor. In this embodiment, the transistors are illustrated as having a rectilinear shape. In other embodiments, a different transistor shape may be employed and/or a different centerline may be selected.

[0017] An upper-most transistor 3a of a primitive group 81 may be offset vertically downward from its associated, respective resistor 5a, and a lower-most transistor 3b of the primitive group 81 may be offset vertically upward from its associated, respective resistor 5b. The amount of vertical offset between each resistor in a primitive group and its respective transistor may be different for each pair or one or more pairs may be offset by different distances. In FIG. 3, for example, the vertical offset D1 is greater than the vertical offset D2 which, in turn, is greater than the vertical offset D3. In an exemplary embodiment, the vertical offsets D1, D2 and D3 may be about 6.5 um, 5.8 um and 5.1 um, respectively. The relative offset may decrease as one moves from the upper and/or lower resistor/transistor pairs toward the center of a primitive group 81. For a transistor near the vertical centerline of a power buss, there may be the smallest vertical offset of the primitive group 81 between a resistor and its associated transistor.

[0018] As a result, adjacent transistors of adjacent primitive groups, for example the upper-most transistor 3a of a primitive group 81 and the lower-most transistor 3b of an adjacent primitive group 81 may be spaced further from each other than spacing of the transistors within either one of the adjacent primitive groups 81. In FIG. 3, for example, an upper-most transistor 3a and a lower-most transistor 3b are spaced, centerline to centerline, a distance V3 apart, the distance V3 being greater than V1. In an exemplary embodiment, the upper-most transistor 3a and a lower-most transistor 3b may be spaced,

centerline-to-centerline, about 100.4 um apart. In an alternative exemplary embodiment, the distance V3 could be less than V1.

[0019] In the exemplary embodiment of FIG. 3, each of the contacts 41 of the transistors 3 in each primitive group 81 are completely covered by and/or enclosed within the perimeter 82 of the area covered by the power buss 8. The power buss 8 may comprise a protective layer over the contacts 41. The power buss 8 may protect the substrate from chemical attack during an etch which may occur during manufacture of the fluid ejection device subsequent to laying down transistor 3, resistors 5 and the busses 8.

[0020] However, only a portion of each of the contacts 41 may be covered by power buss 8. The portion covered needs to be of sufficient to make a reliable electrical path between power buss 8 and contacts 41. The actual area of the covered portion is a function of contact surface area and transistor size.

[0021] An exemplary etch step may be a wet etch using an etchant, which may be TMAH. The etch step may define, in part, an ink feed slot 21 (FIG. 1). In an exemplary embodiment, an ink feed slot may be formed by a process comprising at least two steps. The two steps may be, for example, a wet etch followed by sand blasting. However, other methods and approaches including, but not limited to, laser drilling, drilling, or the like may be used. Without the protective layer, the etchant may attack the substrate through pinholes in a passivation layer over the PSG layer, in the region where the contacts pass through the insulation layer or PSG layer. The etchant may also attack the substrate directly through the contacts. The substrate may be "attacked" in areas of silicon that should not be etched, but which are unintentionally etched during the wet etch process. This may be due to passivation pinholes caused by uniformity and topology issues.

[0022] A power buss 8 may be arranged to cover each of the contacts of each of the transistors in the associated primitive group. The process of covering each of the contacts with a protective layer prior to an etch improved yield over a process in which each of the contacts were not covered by a protective layer.

[0023] The desired, minimum separation between the edges of adjacent power busses to achieve, in order to provide reliable electrical separation of the power busses, may depend on or be limited by the particular photo and etch tooling used in the manufacture of the fluid ejector. In an exemplary embodiment, the vertical distance Y (FIG. 3) between adjacent power busses 8 may be limited to about 8 um. Power buss separation is limited by the photo and etch tooling used in depositing the protective layer. In certain embodiments, an etchant used in the wet etch may remove material from along the edges of the power buss 8. As a result, the spacing between adjacent power busses 8 after the etch may be as much as about 2-4 additional microns larger than the gap prior to the etch. The minimum post-etch gap spacing may therefore be approximately 9.5-10 microns or more in the exemplary embodiment.

[0024] In an exemplary embodiment of a fluid ejection device 1, the vertical spacing or separation distance V1 of the resistors is dependent on the desired print quality as measured in dpi (dots per inch). In an exemplary embodiment, the distance V1 provides a resolution of up to 1200 dpi (1200x2400).

[0025] In FIG. 3, for example, if the upper most transistors 3a and adjacent lower most transistors 3b of adjacent primitive groups 81 were spaced the same distance apart as the resistors 5a and 5b and were not vertically offset from the resistors, some of the contacts would extend into the space Y between the power busses 8. If the space Y were already set as the minimum separation between adjacent power busses, it would not be possible to cover each of the contacts of the upper or lower most contacts with the protective

layer of the power buss 8. If the transistors were simply made narrower, to increase the gap between transistors, efficiency of the transistors may be compromised or desirable efficiencies would not be achieved.

[0026] In the exemplary arrangement of transistors shown in FIG. 3, the transistors 3 within a primitive group 81 are spaced a distance V2 apart, V2 being smaller than the distance V3 between adjacent transistors of adjacent primitive groups 81. This enables a fluid ejection device 1 or printhead die of a given length to accommodate more transistors 3 of a given vertical height H while also providing power busses 8 which cover each of the contacts 41 of the transistors 3 of the associated primitive groups 81.

[0027] In other exemplary embodiments, the vertical spacing of the resistors 5 within a primitive group 81 may not be uniform. The vertical spacing of the transistors 3 of a primitive group 81 may not be spaced uniformly within the primitive group and/or the vertical spacing of the transistors 3 along a column of transistors may not match the spacing of the associated, corresponding resistors 5 along the associated column of resistors. Spacing lower most transistors 3b sufficiently far from upper most transistors 3a between adjacent primitive groups 81 will allow adjacent power busses 8 to be sufficiently separated to provide electrical isolation of the adjacent power busses 8 while providing a protective covering over the contacts 41 of all of the transistors 3 of each primitive group 81. Within the primitive group 81, the transistors may be spaced as close or as far apart as desired. The transistors 3 of a primitive group 81 may be spaced more closely than the associated, respective resistors 5 of the primitive group 81. The spacing of transistors 3 within a primitive group 81 may be closer than the spacing between the lower most transistor of one primitive group and the upper-most transistor of an adjacent primitive group 81. This arrangement or layout of transistors 3 may provide more efficient use of space on the silicon die. The spacing of transistors 3 within one primitive

group 81 may be different from the spacing of transistors 3 within another primitive group 81.

[0028] It is understood that the above-described embodiments are merely illustrative of the possible specific embodiments which may represent principles of the present invention. Other arrangements may readily be devised in accordance with these principles by those skilled in the art without departing from the scope and spirit of the invention.